Secondary-Side Synchronous Rectifier

FEATURES

- Supports CCM, DCM and Quasi-Resonant Topologies
- Original edge opening judgment
- Secondary edge discontinuity judgment
- Supports Low-side/High-side Rectification
- Strong anti-interference ability
- Unique VCC power supply technology
- Support USB-PD+PPS system
- Equipped with chip powered undervoltage protection
- Max 180kHz Switching Frequency
- Fast Turn-off Total Delay of 10ns
- Compatible with Energy Star
- ~150uA Low Quiescent Current
- Few peripheral components

APPLICATIONS

- Chargers for Cell Phones
- AC/DC adapter
- Industrial Power Systems
- Flyback Converters

GENERAL DESCRIPTION

SF6705B is a high-performance secondary synchronous rectification chip with built-in MOS, suitable for isolated synchronous rectification applications, especially suitable for high efficiency requirements in chargers.

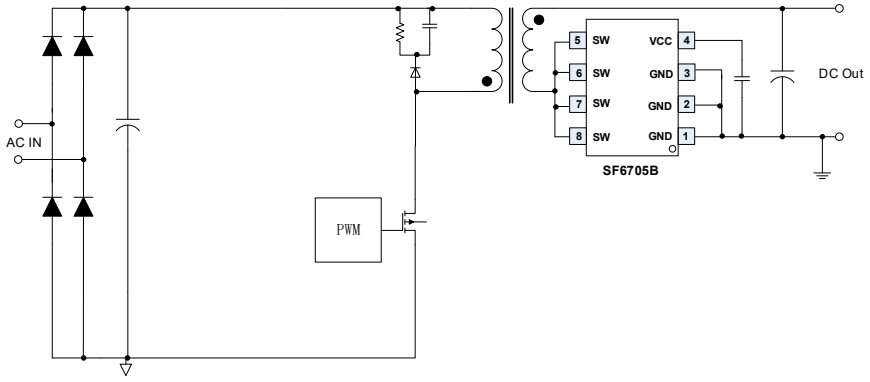
The SF6705B adopts the technology of opening the primary side and intermittent judgment of the secondary side, which can effectively avoid the misoperation of the driving chip caused by excitation oscillation.

The SF6705B adopts a unique VCC power supply technology, which can ensure that the chip will not operate under power in both constant current and constant voltage operating states of the primary control system.

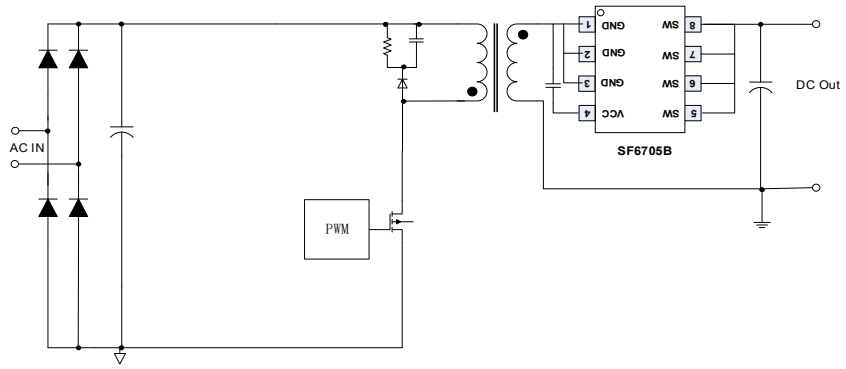
Compatible with CCM, DCM, and QR working modes.

SF6705B is offered in SOP8 package.

TYPICAL APPLICATION

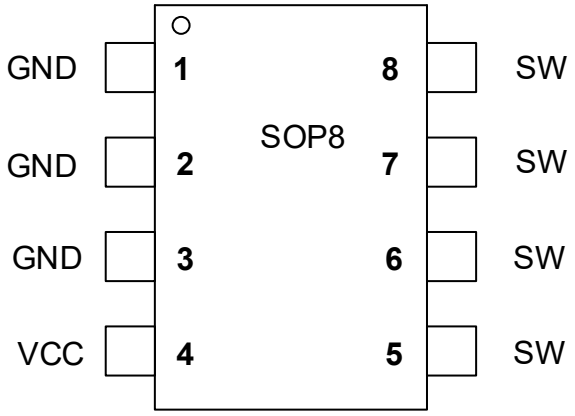


Low-side Rectification



High-side Rectification

Pin Configuration

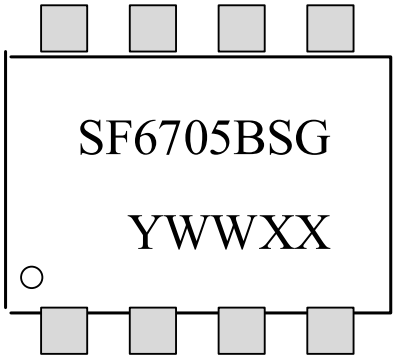


Ordering Information

Part Number	Top Mark	BVdss	Rdson	Package		Tape & Reel
SF6705BSGT	SF6705BSG	45V	15mΩ	SOP8（*）	Green	Yes

（*）MSL(Moisture Sensitivity Level) is level 3. Absorbed moisture could be sensitive to damage during solder reflow, so it's recommended to take floor life into consideration, according to IPC/JEDEC J-SMD-020E(Moisture/Reflow Sensitivity Classification for Non-hermetic Surface Mount Devices).

Marking Information



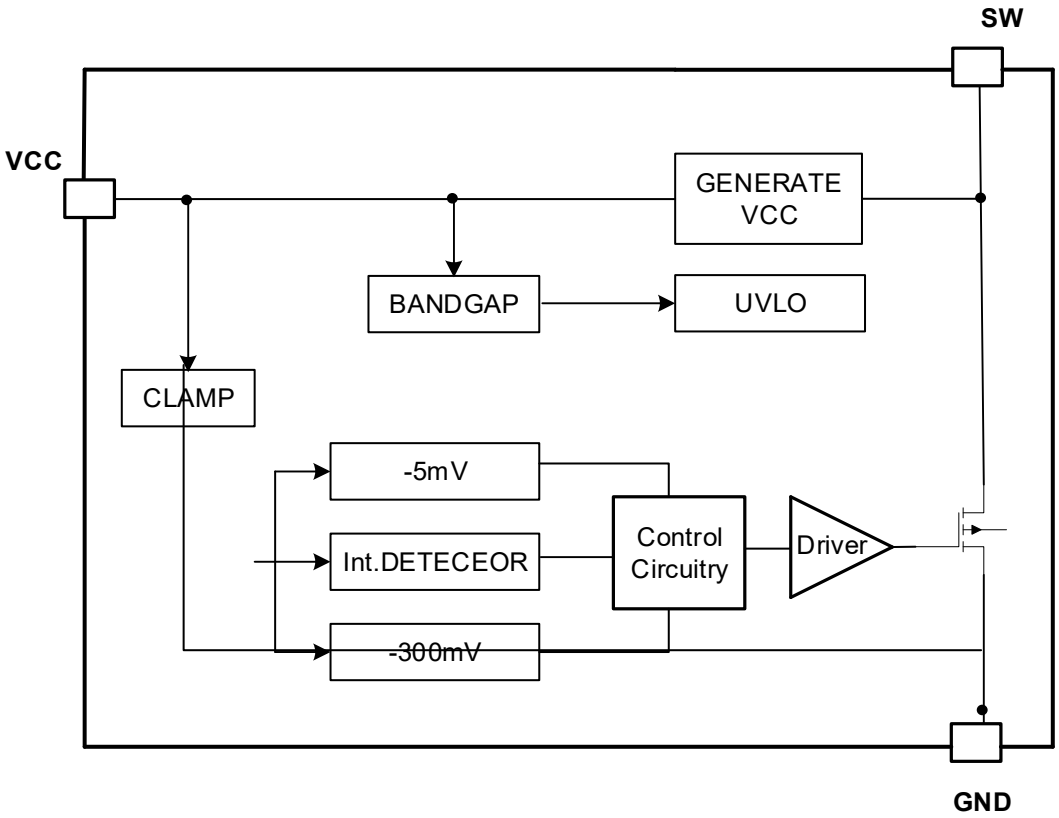
YWW: Year&Week code
XX:Package code and number per week

Pin Description

Pin Num Pin Name I/O Description

1,2,3	GND	P	IC ground pin.
4	VCC	P	Output of internal LDO, it provides bias voltage for the internal circuit and MOSFET driver. Connect this pin to a capacitor
5,6,7,8	SW	P	Drain of internal N-MOS

Block Diagram



Absolute Maximum Ratings (at TA = 25°C)

Characteristics

	Symbol	Rating	Unit
VCC to GND		-0.3 to 12	V
SW to GND		-0.3 to 45V	V
Operating Junction Temperature	T_A	-40 to 150	°C
Storage Junction Temperature	Tstg	-65 to 150	°C

Notes:

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Recommended Operating Range

ELECTRICAL PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNIT
Input Voltage(V_{CC})	5		10	V
hermal Resistance from Junction to case (θ_{JC})		80		°C/W
Thermal Resistance from Junction to ambient (θ_{JA})		160		°C/W

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_{IN}=6.8V, if not otherwise noted)

Characteristics	Symbol		Conditions	Min	Typ	Max	Units
Supply Voltage Section							
V_OP	VCC		self-power		6.8		V
VCC UVLO OFF	VCC_{UVLO_OFF}		VCC drop		3.7		V
VCC UVLO Voltage ON	VCC_{UVLO_ON}		VCC rise		3.9		V
VCC UVLO Hysteresis					0.2		V
I_OP			FSW=65K, load capacitance=2.2nF		2		mA
I_ST			VTH_ON-0.1V		25		uA
Quiescent Current	VCC_{ICQ}		VCC=5.0V，FSW=0	-	150	-	uA
Detection Section							
Turn on Threshold	VTH_ON				-0.3		V
Turn OFF Threshold	VTH_OFF				-5		mV
$TD_{\_ON}$	Ton delay				20		ns
Turn-off Total Delay	Toff_delay				10		ns
T_LEB					1.8		us
Gate Driver Section							
TR_G	rise time		CL=4.7nF		50		ns
TF_G	fall time		CL=4.7nF		50		ns
VG_H	Output High Level		Iload=100mA		6.8		V
VG_L	Output low level		Iload=100mA		0.06		V
$I_{\_GSC}$			Drive source current (peak)		4		A
$I_{\_GSC}$			Drive current (peak)		-5		A
Built-in MOS Section							
Breakdown Voltage	BV_{DSS}	SF6705B	VGS=0V, ID=250μA	45			V
NMOS RDS_{ON}	R_{DS_ON}	SF6705B	VGS=10V, ID=18A		15		mΩ
Gate threshold voltage	VGS(th)	SF6705B	ID=250μA，VDS=VGS	1.2	1.7	2.5	V
Leakage source leakage current	IDSS	SF6705B	VDS=60V，VGS=0V			1	uA
Gate body leakage current	IGSS	SF6705B	VDS=0V, VGS=±20V			±100	nA

OPERATION DESCRIPTION

SF6705B is a high-performance and highly integrated secondary side synchronous rectification controller (upper and lower applications) in a switching power supply system with built-in N-MOSFET. It simulates traditional diode rectifiers and can improve output current capacity and efficiency.

◆ VCC Under voltage lockout(UVLO)

The normal operation of SF6705B depends on the UVLO function implemented on the chip. When the AC power is turned on, the VCC is charged from the secondary winding of the transformer. When the VCC rises above UVLO (off), the IC wakes up and operates normally. Please refer to the timing chart below.

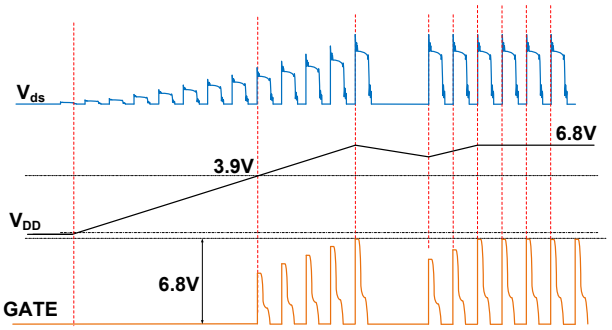


Fig 1 Start Sequence Diagram

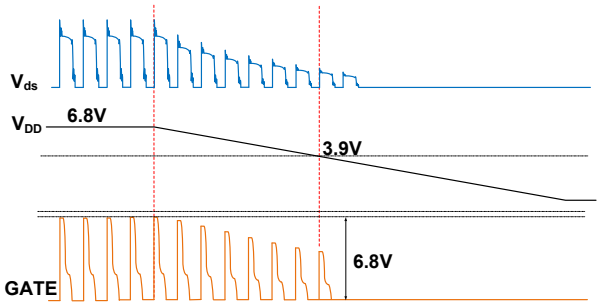


Fig 2 Closing Sequence Diagram

◆ Start

After the system is powered on, the output capacitor is charged through a built-in MOS body diode, and the output voltage rises.

After passing through the internal power supply circuit of the chip, the VCC capacitor is charged. When the voltage of the VCC reaches the opening threshold voltage, the internal control circuit of the chip begins to work, and the MOS conducts and turns off normally.

When MOS conducts normally, current no longer flows through the body diode, but through the MOS channel. When the chip operates normally, the required working current is supplied to the VCC through the VD pin.

◆ Synchronous rectifier tube conduction

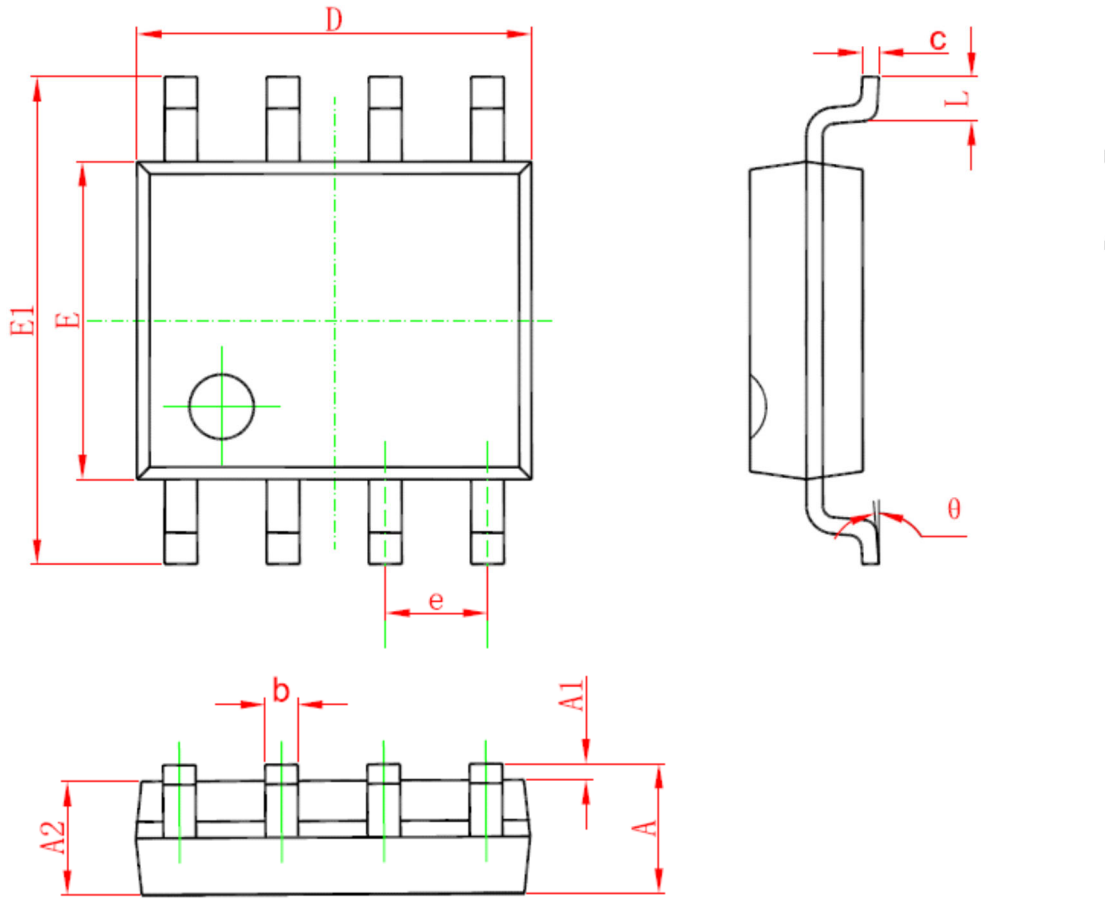
When the flyback converter is in DCM, CCM, or QR operation, Due to the excitation effect of the inductor, oscillation will occur when the primary chip is turned off. In order to prevent false detection of oscillation signals, which may cause abnormal opening of synchronous rectifier tubes, SF6705B adopts patented original side opening judgment technology. When the primary chip is conductive, a flyback voltage is generated between the secondary output GND and the chip GND through a transformer; When the primary chip is turned off, the voltage between the drain D and GND of the secondary SF6705B decreases. SF6705B can accurately determine the opening of the synchronous rectifier by detecting the drop voltage of the drain.

◆Synchronous rectifier tube shutdown

In order to avoid false detection of the shutdown signal caused by large excitation oscillation amplitude during the conduction of the synchronous rectifier tube, SF6705B adopts adaptive minimum shutdown time control to ensure reliable synchronous rectifier operation.

PACKAGE MECHANICAL DATA

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.05 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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