



USB PD 3.2 PROTOCOL AND BUCK CONVERTER HY5334

REVISION 0.5

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R0.5

Page 1 of 18

Table of Contents

1	Features	3	8.4	Line-Drop Compensation	11
2	Applications	3	8.5	NTC Protection.....	11
3	Description.....	3	8.6	Over Voltage Protection	11
4	Typical Application Schematic.....	4	8.7	OCV and Short Protection	11
5	Pin Configurations and Function Descriptions	4	9	Typical Application Circuit	12
6	Specification.....	6	9.1	Dual Port Application	12
6.1	Absolute Maximum Ratings.....	6	9.2	Single Port Application.....	13
6.2	Thermal Information	6	9.3	2C1A Fix Power Shared Application.....	14
6.3	Recommended Operating Conditions	6	9.4	2C1A Smart Power Shared Application.....	15
6.4	Electrical Characteristics.....	7	10	Mechanical, Packaging & Orderable Info	16
7	Function Description.....	9	10.1	Package Outline: QFN 4mm X 4mm - 32L..	16
7.1	Overview	9	10.2	Ordering Information.....	17
7.2	Function Block	10	10.3	Tape and Reel Information.....	17
8	Application Notes.....	11	10.4	Marking and Date Code Information	17
8.1	VIN PIN & VOUT PIN & VCC PIN.....	11	12	Important Notice.....	18
8.2	MP PIN.....	11	13	Contact Information	18
8.3	VOUT1 VBUS1 & VOUT2 VBUS2	11			

List of Figures

Fig. 1.	Typical Application Schematic	4
Fig. 2.	Packages Top View.....	4
Fig. 3.	Function Block	10
Fig. 4.	NTC Protection	11
Fig. 5.	Typical Application.....	12
Fig. 6.	Typical Application.....	13
Fig. 7.	Typical Application Diagram	14
Fig. 8.	Typical Application Diagram	15
Fig. 9.	Package Outline.....	16

List of Tables

Table 1.	Pin Function Descriptions	4
Table 2.	Absolute Maximum Ratings	6
Table 3.	Recommended Operating Conditions.....	6
Table 4.	Electrical Characteristics	7
Table 5.	Dual Port Application BOM list	12
Table 6.	Single Port Application BOM list	13

BUCK CONVERTER AND Dual Ports Controller

1 Features

- USB Type-C 2.2 and USB PD 3.2 / 2.0 Compliant
 - Support 7 Programmable PDOs
 - Support AVS
 - Support USB Type-C 2.2 DFP
 - Support eMarker Detection
- Support UFCS
 - Support 3 Programmable Num
- Support BC1.2 DCP and HVDCP Protocols
 - QC2.0 / QC3.0 / QC3.0+ Class A or Class B
 - Huawei FCP / SCP
 - Samsung AFC
 - Apple 2.4 A
 - BC1.2 DCP
 - PE+ 1.1 / 2.0
- Safety Integration
 - Over voltage protection
 - Over current protection
 - Peak current protection
 - Over-temperature Protection
 - CC1 / CC2 / DP / DM overvoltage protection
 - NTC
 - UVLO
- Integration Buck Regulator
 - 5V to 35V Input Voltage Range
 - 3.3V to 21V Output Voltage Range
 - COT Control Mode
 - Support CC/CV Mode
 - Maximum Duty Cycle 98%
 - Support max 5A output current
 - As low as 500uA standby current at 12V input
- Support External I2C
- Integration discharge
- As low as 10 mA light load detection
- Programable Cable drop compensation
- Adaptive power control by Temperature
- Support Dual Chip Power Link
- Support Online Update
- HBM ESD ± 4 kV rating for all pins
- QFN 4mm x 4mm-32L

2 Applications

- Adaptor

- Power Strip

3 Description

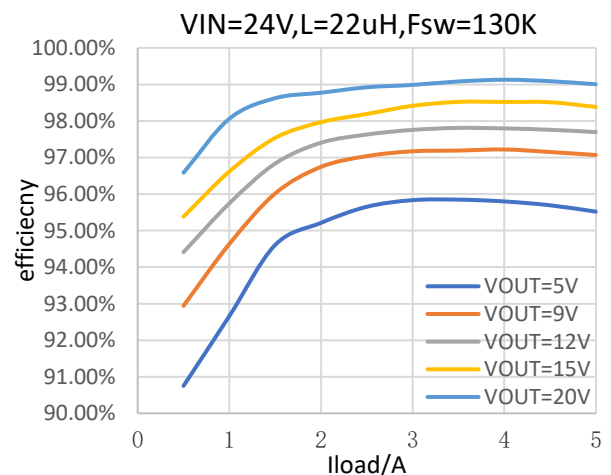
The HY5334 is a high performance, high integration Buck Converter and Dual Ports Controller. Internal integration of 5A high-efficiency synchronous buck converter. The HY5334 support 7 PDOs with programmable current and voltage which are fully compliant with USB Power Delivery Specification Revision 3.2, Version 1.0. Besides, the HY5334 also supports BC1.2 DCP, Apple 2.4A, QC2.0 / QC3.0 / QC3.0+, AFC, FCP, SCP, UFCS and PE+ 1.1 / 2.0 protocols.

The HY5334 designed for Dual Ports controller, which can easily use to 2C or 1C1A application. Each port operates independently in fast charging mode and power is shared when both ports-working.

The HY5334 integrates Chip-Link technology, making it easy to achieves Dual Ports application.

The HY5334 integrates perfect protection such as Over Voltage Protection (OVP), Under Voltage Lockout (UVLO), Over Current Protection (OCP), CC or DP DM Over Voltage Protection and Over-temperature Protection.

The HY5334 is available in QFN 4mm x 4mm-32L package.



4 Typical Application Schematic

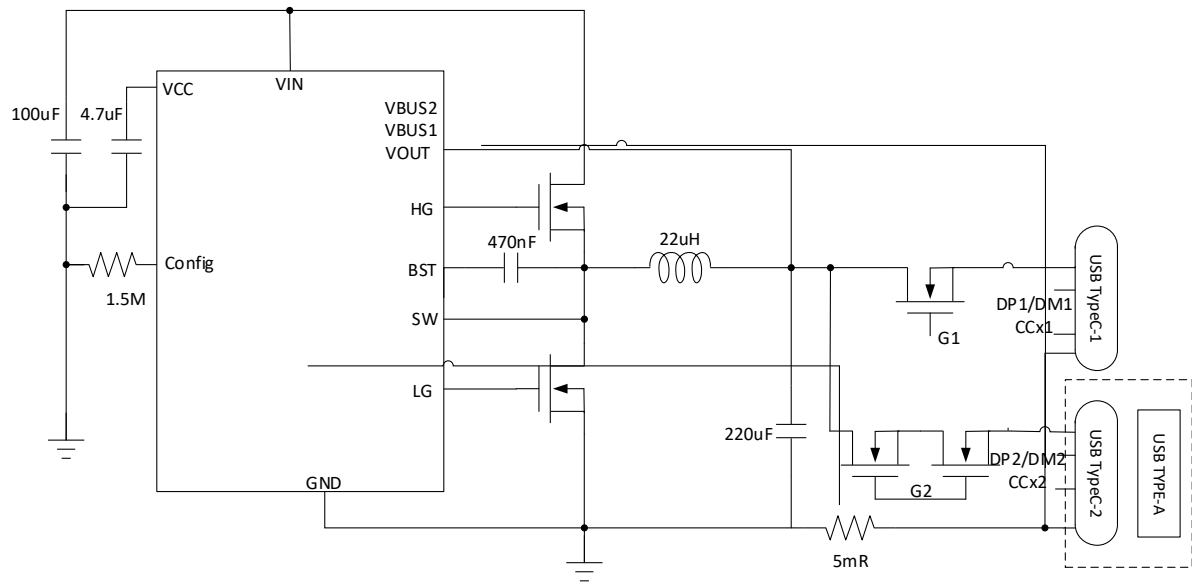
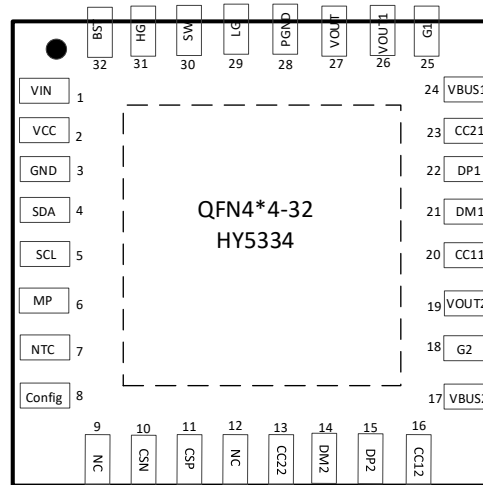


Fig. 1. Typical Application Schematic

5 Pin Configurations and Function Descriptions



QFN 4mm x 4mm-32L

Fig. 2. Packages Top View

Table 1. Pin Function Descriptions

Pin	Name	Description
1	VIN	Power supply for internal circuits
2	VCC	Internal LDO output, Connect 4.7uF Capacitance to GND
3	GND	Ground

4	SDA	I2C Data Terminal
5	SCL	I2C Clock Terminal
6	MP	Communication with another chip through this pin if Power link function enable. If not used must tie to GND net
7	NTC	An external negative temperature coefficient resistor connected to this pin for remote temperature sensing
8	Config	Debug Pin, Connect the 1.5M resistor to the ground.
10	CSN	Current detection negative point and current output
11	CSP	Current detection positive point and current input
13	CC22	USB Type-C2 CC2
14	DM2	USB Type-C2 DM
15	DP2	USB Type-C2 DP
16	CC12	USB Type-C2 CC1
17	VBUS2	Type-C2 Light Load Detect Pin, Connect to Type-C2 MOS Source Terminal
18	G2	Type-C2 MOS Gate Driver
19	VOOUT2	Type-C2 Light Load Detect Pin, Connect to Type-C2 MOS Drian Terminal
20	CC11	USB Type-C1 CC1
21	DM1	USB Type-C1 DM
22	DP1	USB Type-C1 DP
23	CC21	USB Type-C1 CC2
24	VBUS1	Type-C1 Light Load Detect Pin, Connect to Type-C1 MOSFET Source Terminal
25	G1	Type-C1 MOS Gate Driver
26	VOOUT1	Type-C1 Light Load Detect Pin, Connect to Type-C1 MOSFET Drian Terminal
27	VOUT	DCDC VOUT Sense
28	PGND	Low Side Sense, Connect to Low-Side MOSFET Source
29	LG	Connect to the gate of the low-side synchronous MOSFET through a short, low inductance path
30	SW	Switch node. Connect to the negative terminal of the bootstrap capacitor and the source terminal of the high-side MOSFET
31	HG	Connect to the gate of the high-side synchronous MOSFET through a short, low inductance path
32	BST	High-side driver supply for bootstrap gate drive

6 Specification

6.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Unit
BST	-0.3	45	V
HG-SW	-0.3	5	V
G1-VBUS1, G2-VBUS2	-0.3	6	V
CSN, CSP, NTC, MP, LG	-0.3	6.5	V
VIN, VOUT, VOUT1, VOUT2, SW	-0.3	40	V
CC11, CC21, CC12, CC22, DP1, DM1, DP2, DM2, VBUS1, VBUS2	-0.3	26	V
Junction Temperature Range	-40	150	°C
Ambient Temperature Range	-40	150	°C
Storage Temperature Range	-55	150	°C
Lead Temperature Range (Soldering 10 sec)		260	°C
ESD Human Body Model (100 pF Capacitance, Series 1.5 KΩ)	-4000	+4000	V

Note: Exceeding the specified limits for the operating conditions of the device can result in permanent damage to the device. The parameters provided are only the limit values for the operating conditions, and operating the device outside of the recommended working conditions is not advisable. The device's reliability may be affected by prolonged operation under extreme conditions.

6.2 Thermal Information

Table 3. Thermal Information

Sym.	Thermal Metric	Value	Unit
R_{θ_JA}	Junction-to-ambient thermal resistance ^{1 2}	47	°C/W
$R_{\theta_JC_TOP}$	Junction-to-case (top) thermal resistance	40	°C/W

Note: The maximum allowable power dissipation is a function of the maximum junction temperature $T_{\theta_JCT_MAX}$, the junction-to-ambient thermal resistance R_{θ_JA} , and the ambient temperature T_{θ_AMB} . The maximum allowable continuous power dissipation at any ambient temperature is calculated by:

$$P_{DSSP_MAX} = \frac{T_{\theta_JCT_MAX} - T_{\theta_AMB}}{R_{\theta_JA}}$$

Equation 1

Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

6.3 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Min	Max	Unit
Input Voltage VIN	5	35	V
Junction Temperature Range	-40	150	°C

¹ The package thermal impedance is calculated in accordance with JESD 51-7.

² Thermal Resistances were simulated on a 4-layer, JEDEC board.

6.4 Electrical Characteristics

$V_{in} = 5\text{ V}$, $T_{AMB} = 25\text{ }^{\circ}\text{C}$ (unless noted otherwise)

Table 4. Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
DCDC						
V_{IN}	Input Voltage		5		35	V
V_{IN_UVLO}		Rising		4.7		V
$V_{IN_UVLO_HYS}$	Input Under-Voltage Lockout (UVLO)			0.2		V
I_Q	Input Quiescent Current	CC Locked, $V_{in}=12\text{V}$		2		mA
		CC Unlocked, $V_{in}=12\text{V}$		500		uA
V_{CC}	Internal LDO Output			5		V
I_{CC_MAX}	Max Output Current of VCC	$V_{IN}=12\text{V}$		20		mA
I_{HG_Peak}	Gate Pull Up	$V_{BST}-V_{SW}=5\text{V}$		120		mA
	Gate Pull Down			400		mA
I_{LG_Peak}	Gate Pull Up	$V_{CC}=5\text{V}$		120		mA
	Gate Pull Down			800		mA
f_{SW}	Switching Frequency	$R_{config}=1.5\text{M}$		130		KHZ
D_{MAX}	Maximum Duty Cycle			98		%
VOUT						
V_{OVP_TH}	$V_{OUT} = 5\text{V}$	For fixed PDO. For the continuous mode, it will select the threshold based on the range		6		V
	$V_{OUT} = 9\text{V}$			10.5		V
	$V_{OUT} = 12\text{V}$			13.8		V
	$V_{OUT} = 15\text{V}$			17.8		V
	$V_{OUT} = 20\text{V}$			24		V
R_{VBUS}	Bleeding resistor			100		k Ω
BMC Transmitter (CC1, CC2)						
z_{Driver}	TX Output Impedance		30	54	70	Ω
V_{Swing}	BMC Amplitude		1.050	1.125	1.200	V
V_{TXLOW}	Transmit LOW				75	mV
$f_{BitRate}$	BMC Rate		270	300	330	kbps
BMC Receiver (CC1, CC2)						
V_{RXHI}	Receiver HIGH	Rising edge		840		mV
V_{RXLOW}	Receiver LOW	Falling edge		530		mV
Type-C DFP specification (CC1, CC2)						
V_{D_SRC3A}	Detach threshold when detached in 3A DFP mode	Rising threshold	2.5	2.625	2.75	V
		Hysterias		0.05		V
V_{Rd_SRC3A}	R_a, R_d detection threshold in 3A mode (falling)	$0\text{V} \leq V_{CCx} \leq 2.5\text{V}$	0.75	0.79	0.83	V
		Hysterias		0.02		V
I_{RP_SRC}	CC1/CC2 Broadcasting current	3A DFP, $R_D=5.1\text{K}$	1.6	1.68	1.76	V
$T_{CCDebounce}$	Deglintch filter for UFP attach detection		120	150	180	ms
$T_{PDDebounce}$	Deglintch filter for UFP detach detection		12	15	18	ms
Constant Current						
CC	Constant current point	Configurable				
OCP	Short current protection			16		A

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
HVDCP interface (DP, DM)						
V _{DAT_REF}	Data threshold voltage		0.25	0.325	0.4	V
T _{DP_DEGLTICH_HIGH}	Denounce time for DP high detection			1.1		s
T _{DM_DEGLTICH_LOW}	Denounce time for DM low detection			1		ms
T _{VOUT_CHG}	Denounce time for VOUT variation		20	40	60	ms
R _{DP_LKG}	DP Leakage resistor			650		kΩ
R _{DM_DWN}	DM Pull down resistor			20		kΩ
V _{TH_PD}	Device connection threshold		0.25	0.325	0.4	V
T _{DPD}	Debounce time for device connection detection		120	160	200	ms
ΔI _{UP}	Voltage step up current	R1= 100kΩ		0.2		μA
ΔI _{DOWN}	Voltage step down current	R1= 100kΩ		0.2		μA
T _{DUR_STEP}	Step time for continuous mode	QC3.0 mode		120		μs
Apple 2.4A Mode						
V _{DAT_2P7}	VDP/VDM	Apple 2.4A mode Voltage	2.57	2.7	2.84	V
UFCS mode						
V _{U_TX_VOH}	UFCS TX valid high		2.56	3.3	3.6	V
V _{U_TX_VOL}	UFCS TX valid low				0.5	V
V _{U_RX_VOH}	UFCS RX valid high		1.4			V
V _{U_RX_VOL}	UFCS RX valid low				0.99	V
FCP mode						
V _{TX_VOH}	DM FCP TX valid high		1.8			V
V _{TX_VOL}	DM FCP TX valid low				0.3	V
V _{RX_VOH}	DM FCP RX valid high			1.2		V
V _{RX_VOL}	DM FCP RX valid low			0.9		V
UI	Unit interval for PHY	F _{CLK} = 125 kHz	144	160	176	μs
NTC						
I _{NTC}	NTC source current			48		μA
V _{NTC_TH}	NTC Protection Threshold	Rising		0.6		V
		Falling		0.3		V
V _{NTC_HYS}		Hysterias		0.3		V
OTP						
T _{J1}	Over temperature protection	Rising edge		145		°C
		Hysteresis		20		°C

7 Function Description

7.1 Overview

The HY5334 is a high performance, high integration Buck Converter and Dual Ports Controller. Internal integration of 5A high-efficiency synchronous buck converter. The HY5334 support 7 PDOs with programmable current and voltage which are fully compliant with USB Power Delivery Specification Revision 3.2, Version 1.0. Besides, the HY5334 also supports BC1.2 DCP, Apple 2.4A, QC2.0 / QC3.0 / QC3.0+, AFC, FCP, SCP, UFCS and PE+ 1.1 / 2.0 protocols. It is an ideal solution for power supply devices liking car chargers, quick charger adapters, and smart power strips.

The HY5334 high voltage switching regulator features all of the functions necessary to implement an efficient high voltage buck regulator using a minimum of external components. This easy to use regulator integrates high-side and low-side MOSFET drivers capable of supplying output currents of 5A. The operating frequency is 130 kHz(Rconfig=1.5M).

The HY5334 integrates the CV and CC loop control. When the load current is below to CC current limit, the Circuit output constant voltage. When the load current reaches the CC current limit, the output current will be limited to this value, and the output voltage will be decreased.

The HY5334 designed for Dual ports controller, which can easily use to 2C or 1C1A application. Each port operates independently in fast charging mode and power is shared when both ports-working.

The output voltage of the HY5334 has a programmable line compensation function. After the output current increases, the output voltage will be correspondingly increased to compensate for the voltage drop caused by the connection line impedance. For specific configuration requirements, please contact HYASiC.

The HY5334 has multiple protection functions, including output over-voltage protection, data pin short circuit protection, over-current protection and over-temperature protection.

7.2 Function Block

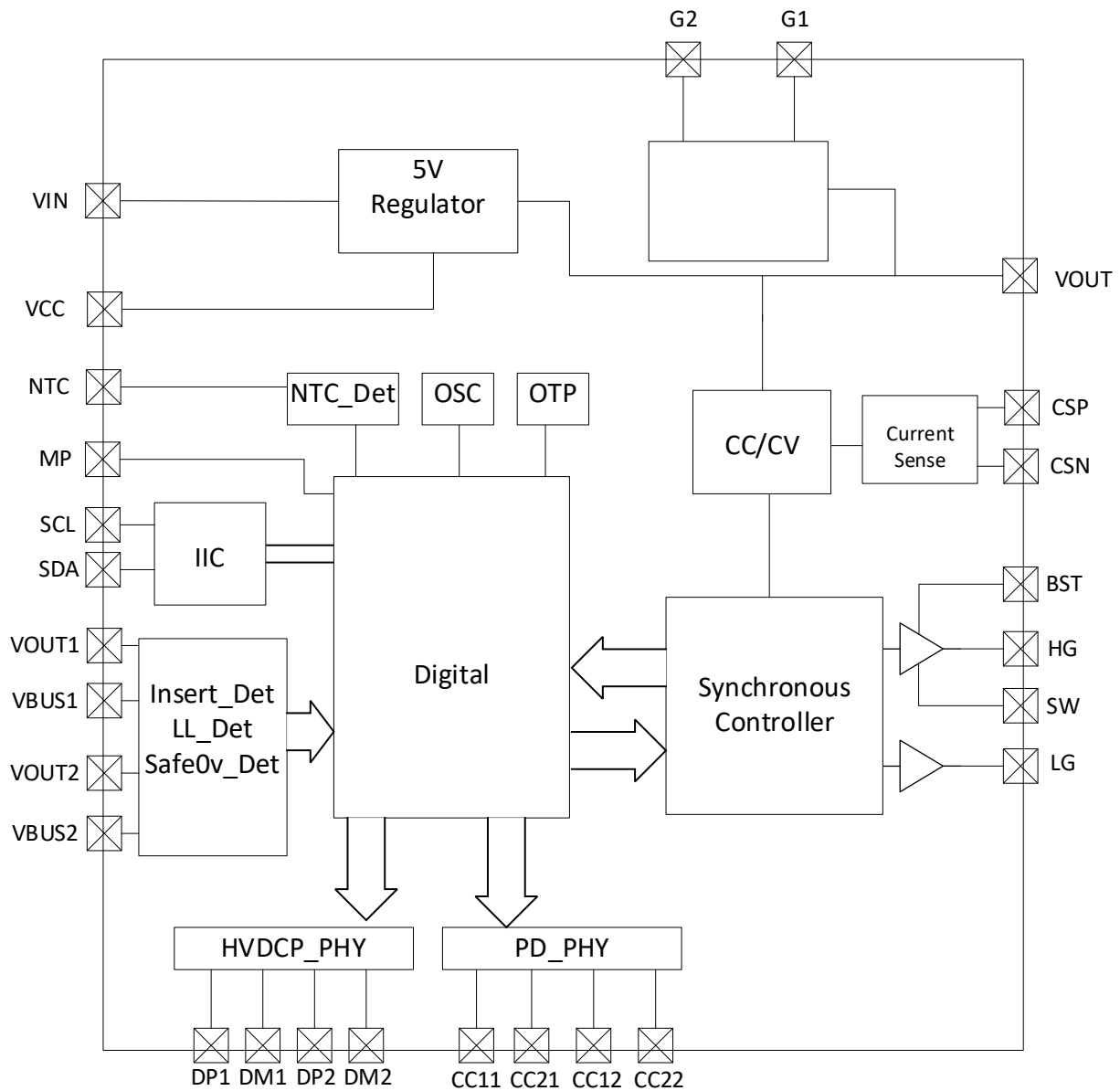


Fig. 3. Function Block

8 Application Notes

8.1 VIN PIN & VOUT PIN & VCC PIN

The VIN pin and VOUT pin is the chip's internal power supply input and voltage sense input. VIN connected to the DC source and connect 100uF Capacitance to GND. The VOUT pin is DCDC output feedback and safe-5V sense terminal.

The VCC pin is internal LDO output, connect 1uF capacitance to GND.

8.2 MP PIN

This pin is used to perform communication between two chips if Chip-Link function enable.

8.3 VOUT1 VBUS1 & VOUT2 VBUS2

The VOUTx and VBUSx sense Type-C MOSFET Voltage drop to detect light load. The VOUTx close to MOSFET Drain and the VBUSx close to MOSFET source.

8.4 Line-Drop Compensation

The Built-in line drop compensation function of the HY5334 has programmable compensation coefficient to meet different application, according to output current. The HY5334 currently supports five types of line drop compensation coefficients: 0 mV/A, 50 mV/A, 100 mV/A, 150 mV/A, 200 mV/A. The default configuration is 100 mV/A.

8.5 NTC Protection

The HY5334 uses the NTC pin to sense the external temperature. As show in Fig.5, there is an internal current source 48 μ A at the NTC pin. With an external NTC resistor from NTC pin to ground, the HY5334 can detect the voltage across this NTC resistor and calculate the temperature per the T-R characteristics. When the NTC PIN is used to power reduction function, the threshold is 0.6 V, when it used to protection function, the rising threshold is 0.6 V and the falling threshold 0.3 V.



Fig. 4. NTC Protection

8.6 Over Voltage Protection

The HY5334 supports OVP by monitoring the voltage of VOUT pin, once the voltage exceeds the over voltage threshold of the required the OVP procedure will be triggered, and then the HY5334 turns off NMOS FET quickly.

8.7 OCP and Short Protection

The HY5334 monitors output current through the sense resistor connected to CSN and CSP for over current and short-circuit protection. When the output current exceeds the over current protection threshold or short-circuit protection threshold corresponding to the requested, the over current or short-circuit protection procedure is triggered, and then the HY5334 turns off NMOS FET quickly.

9 Typical Application Circuit

9.1 Dual Port Application

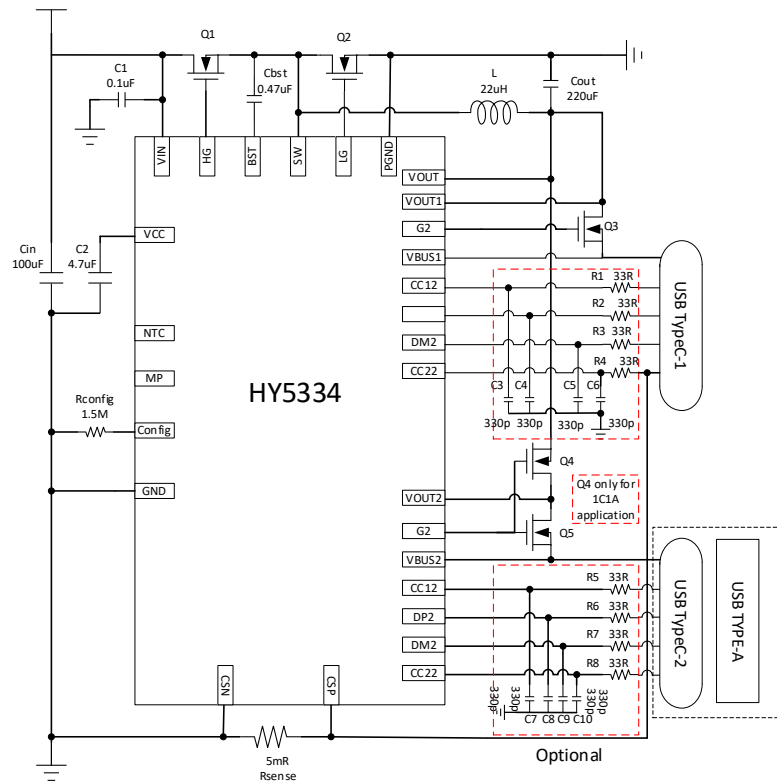


Fig. 5. Typical Application

Note: 1, Must using Kelvin Connect to connect current sense resistor Rsense.

2, If the TVS adds to CC pin, it must exceed 7V.

Table 5. Dual Port Application BOM list

No.	Part Name	Description	Unit	Qty	Location
1	IC	HY5334	PCS	1	
2	SMD capacitor	0603, 4.7uF, +/-20%, 25V, X5R	PCS	1	C2
3	SMD capacitor	0603, 100nF, +/-20%, 25V, X5R	PCS	1	C1
4	SMD capacitor	0603, 0.47uF, +/-20%, 25V, X5R	PCS	1	Cbst
5	SMD capacitor	0603, 330pF, +/-20%, 25V, X5R, for option	PCS	8	C3~C10
6	SMD resistor	0603, 1.5M, 1%	PCS	1	Rconfig
7	SMD resistor	0603, 33R, 5%, for option	PCS	8	R1~R8
8	Inductor	22uH, power inductor	PCS	1	L1
9	capacitor	100uF/35V	PCS	1	Cin
10	capacitor	220uF/25V	PCS	1	Cout
11	NMOS	Choose based on application	PCS	5	Q1~Q5
12	SMD resistor	1206, 5mR, 1%	PCS	1	Rsense

9.2 Single Port Application

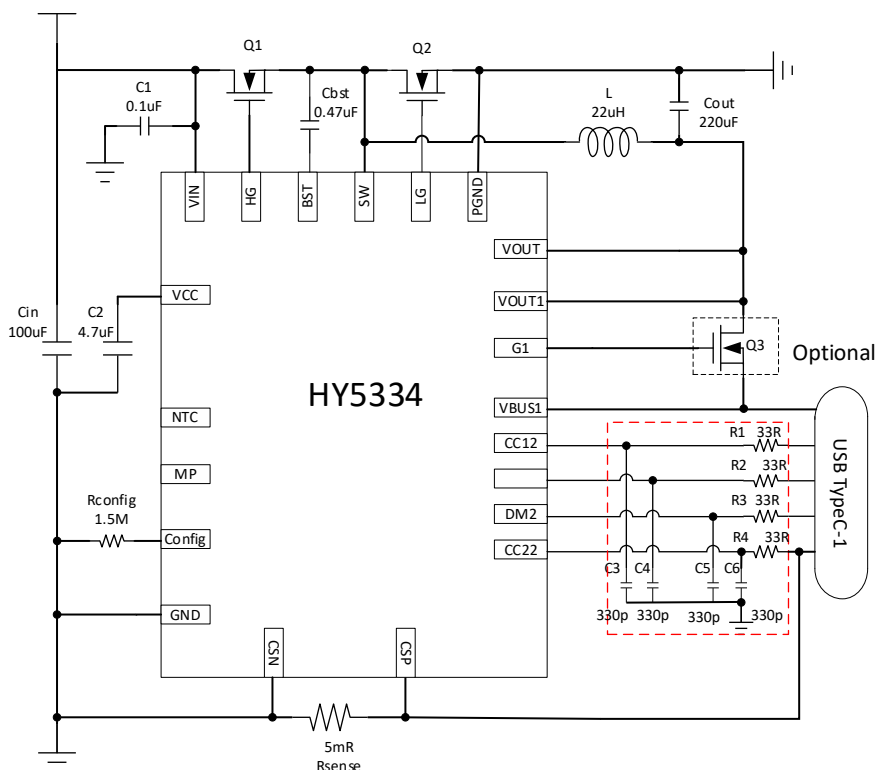


Fig. 6. Typical Application

Note: 1, Must using Kelvin Connect to connect current sense resistor Rsense.

2, If the TVS adds to CC pin, it must exceed 7V.

3, When Q3 not used, the VBUS1, VOUT1 and G2 Pin should be set to floating.

Table 6. Single Port Application BOM list

No.	Part Name	Description	Unit	Qty	Location
1	IC	HY5334	PCS	1	
2	SMD capacitor	0603, 4.7uF, +/-20%, 25V, X5R	PCS	1	C2
3	SMD capacitor	0603, 100nF, +/-20%, 25V, X5R	PCS	1	C1
4	SMD capacitor	0603, 0.47uF, +/-20%, 25V, X5R	PCS	1	Cbst
5	SMD capacitor	0603, 330pF, +/-20%, 25V, X5R, for option	PCS	8	C3~C10
6	SMD resistor	0603, 1.5M, 1%	PCS	1	Rconfig
7	SMD resistor	0603, 33R, 5%, for option	PCS	8	R1~R8
8	Inductor	22uH, power inductor	PCS	1	L1
9	capacitor	100uF/35V	PCS	1	Cin
10	capacitor	220uF/25V	PCS	1	Cout
11	NMOS	Choose based on application (Q3 for option)	PCS	3	Q1~Q3
12	SMD resistor	1206, 5mR, 1%	PCS	1	Rsense

9.3 2C1A Fix Power Shared Application

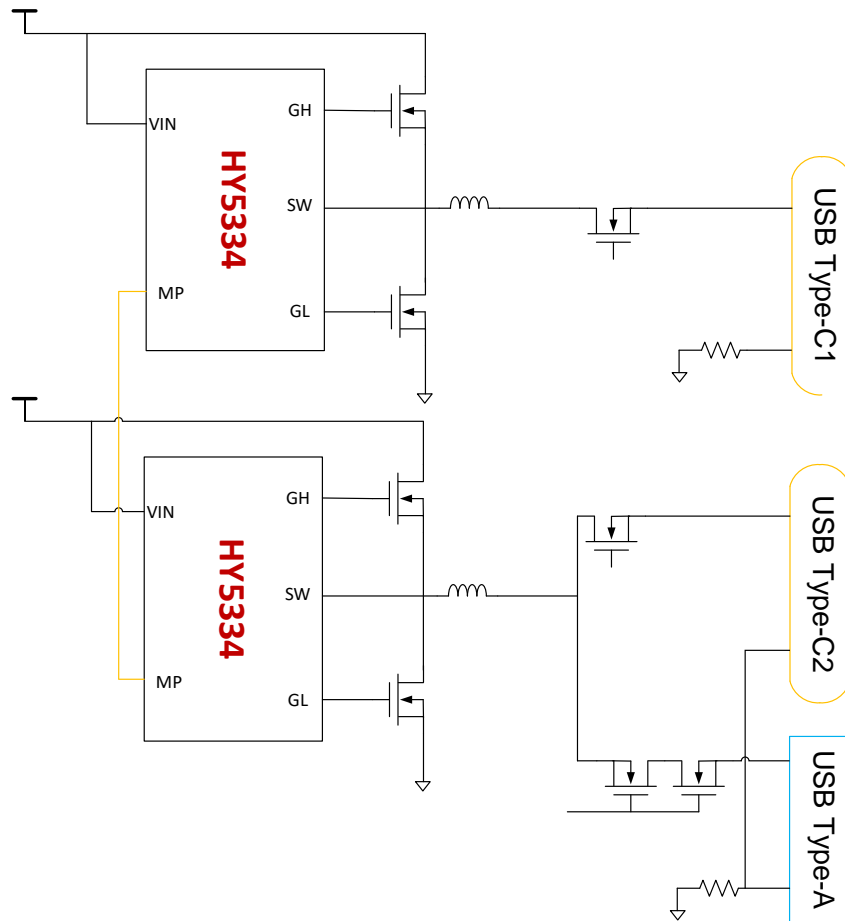


Fig. 7. Typical Application Diagram

The following are instructions for 65 W down 30 W application:

- 1、 When any port is working, it can charge quickly (65 W for port C or 20 W for port A).
- 2、 When chip 1 and one port of chip 2 are working, they can both charge quickly (30 W for port C or 20 W for port A).
- 3、 When chip 1 work and two ports of chip 2 works, chip 2 shares the power of 5V/3A, but chip 1 still charges quickly (30 W).

9.4 2C1A Smart Power Shared Application

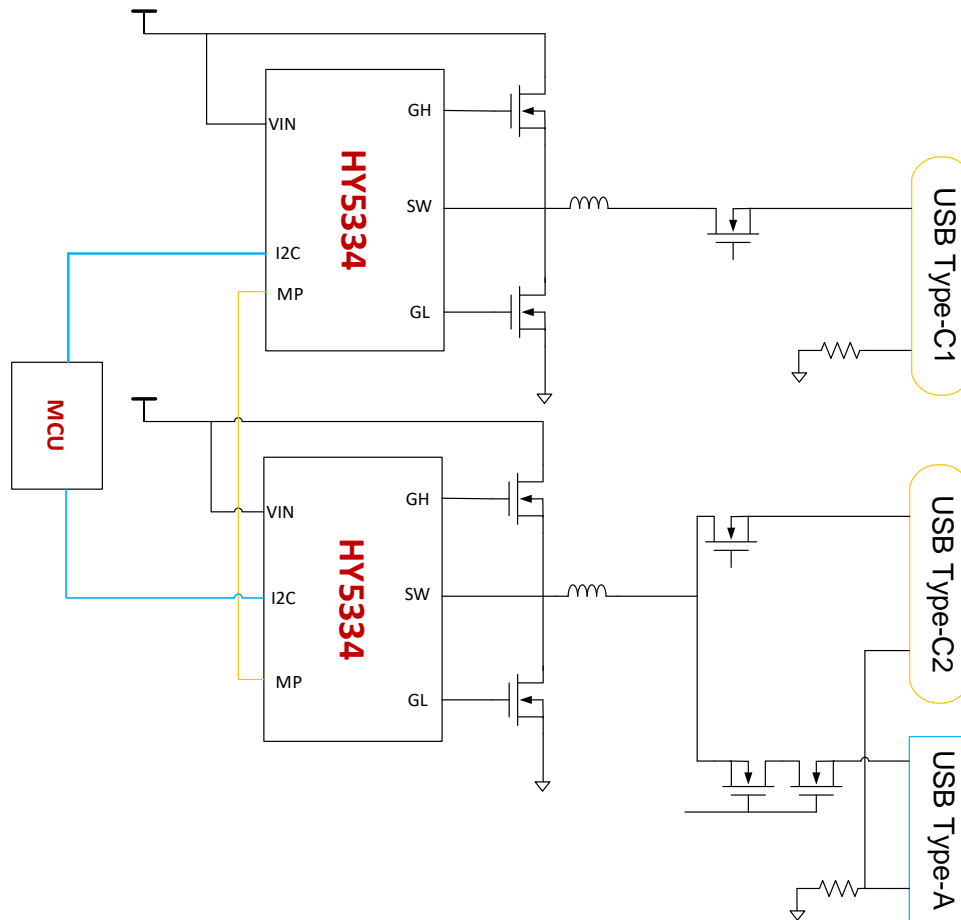


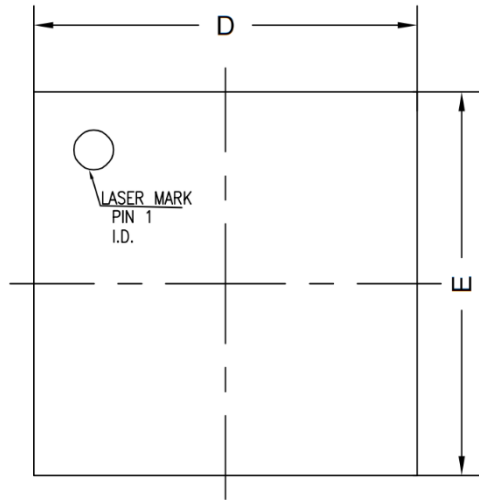
Fig. 8. Typical Application Diagram

The following are instructions for 65W application:

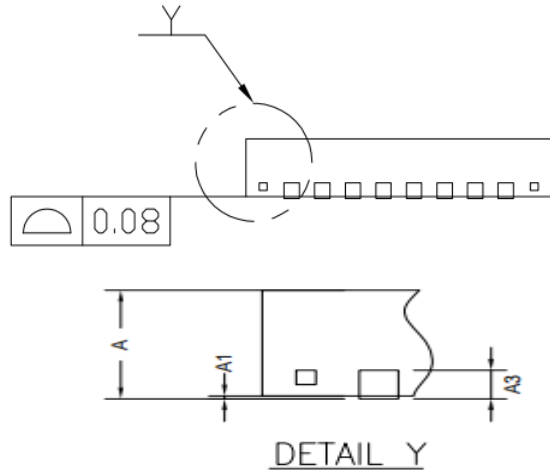
1. When any port is working, it can full charge power for 100W.
2. When port C1 operates at 65W, the port C2 operates at 30W, when port C1 operates at 30W, the port C2 operates at 65W.
3. When C1 port operates at 65W, the port A operates at 30W, when C1 port operates at 30W, the C2 port operates at 65W

10 Mechanical, Packaging & Orderable Info

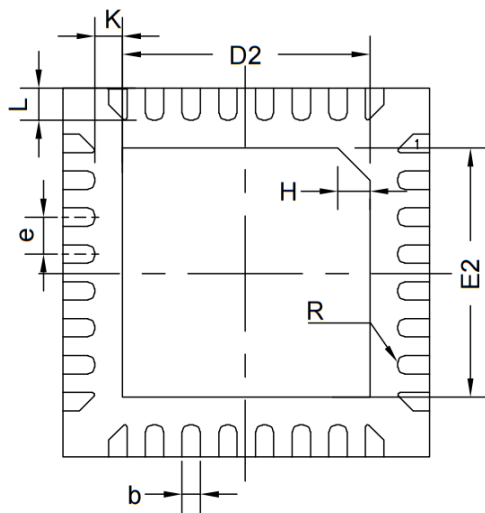
10.1 Package Outline: QFN 4mm X 4mm - 32L



Top View



Side View



Bottom View

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e	0.40BSC		
K	0.30REF		
H	0.35REF		
L	0.275	0.35	0.425
R	0.075REF		

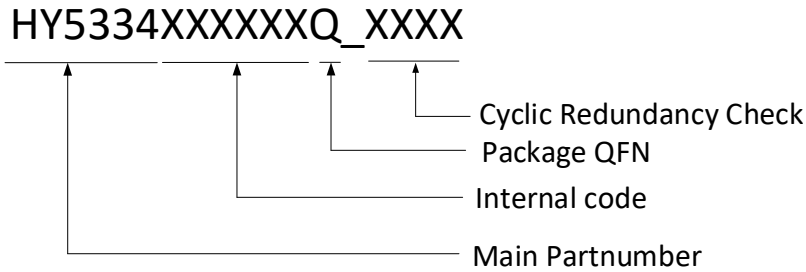
Legend

QFN 4mm X 4mm - 32L

Fig. 9. Package Outline

10.2 Ordering Information

Part Number	Configuration	Package	MOD



Note:

- 1, The Cyclic Redundancy Check (CRC) will be changed by software update.
- 2, The Internal code is defined by the first sample.

10.3 Tape and Reel Information

Package Type	PCs/Reel	Reel/Reel Box	Reel Box/Carton Box	PCs/Carton Box
QFN 4X4-32L	6k	1	5	30k

10.4 Marking and Date Code Information



HY5334
 Product Mark
 A BC XX
 Year Code Week Code Internal Code

Year		Year Code
2009	2024	A
2010	2025	B
2011	2026	C
2012	2027	D
2013	2028	E
2014	2029	F
2015	2030	G
2016	2031	H
2017	2032	J
2018	2033	K
2019	2034	L
2020	2035	M
2021	2036	N
2022	2037	P
2023	2038	Q

12 Important Notice

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13 Contact Information