HYASiC
Digital Power ASIC

USB TYPE-C AND USB TYPE-A MULTI PORTS CONTROLLER

HY5324

REVISION 1.0

DOCUMENTATION NUMBER:
DS_HY5324_R1.0

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USB 1C2A Multi Ports Controller

1 Features

- USB Type-C 2.2 and USB PD 3.1/2.0 Compliant
  - Support 7 Programmable PDOs
  - Support USB Type-C 2.2 DFP
- Support UFCS
  - Support 5 Programmable Nums
- Support BC1.2 DCP and HVDCP Protocols
  - QC2.0/QC3.0/QC3.0+ Class A or Class B
  - Huawei FCP/SCP
  - Samsung AFC
  - Apple 2.4A
  - BC1.2 DCP
  - PE+1.1/2.0
- Safety Integration
  - Over voltage protection
  - Over current protection
  - Output short protection
  - Over-temperature Protection
  - CC1/CC2/DP/DM overvoltage protection
  - NTC
  - UVLO
- External N-MOSFET Supported
- Support External 5mΩ current sense
- As low as 10 mA light load detection
- Integration discharge
- Programable Cable drop compensation
- Support Constant Current and Constant Voltage Loop
- Adaptive power control by Temperature
- Single sense resistor for 1C2A application
- Support Dual Chip Power-Link
- Support External I2C
- Support Online Update
- HBM ESD ±4kV rating for all pins
- QFN-32L (4 mmx4 mm)

2 Applications

- Adaptor
- Power Strip

3 Description

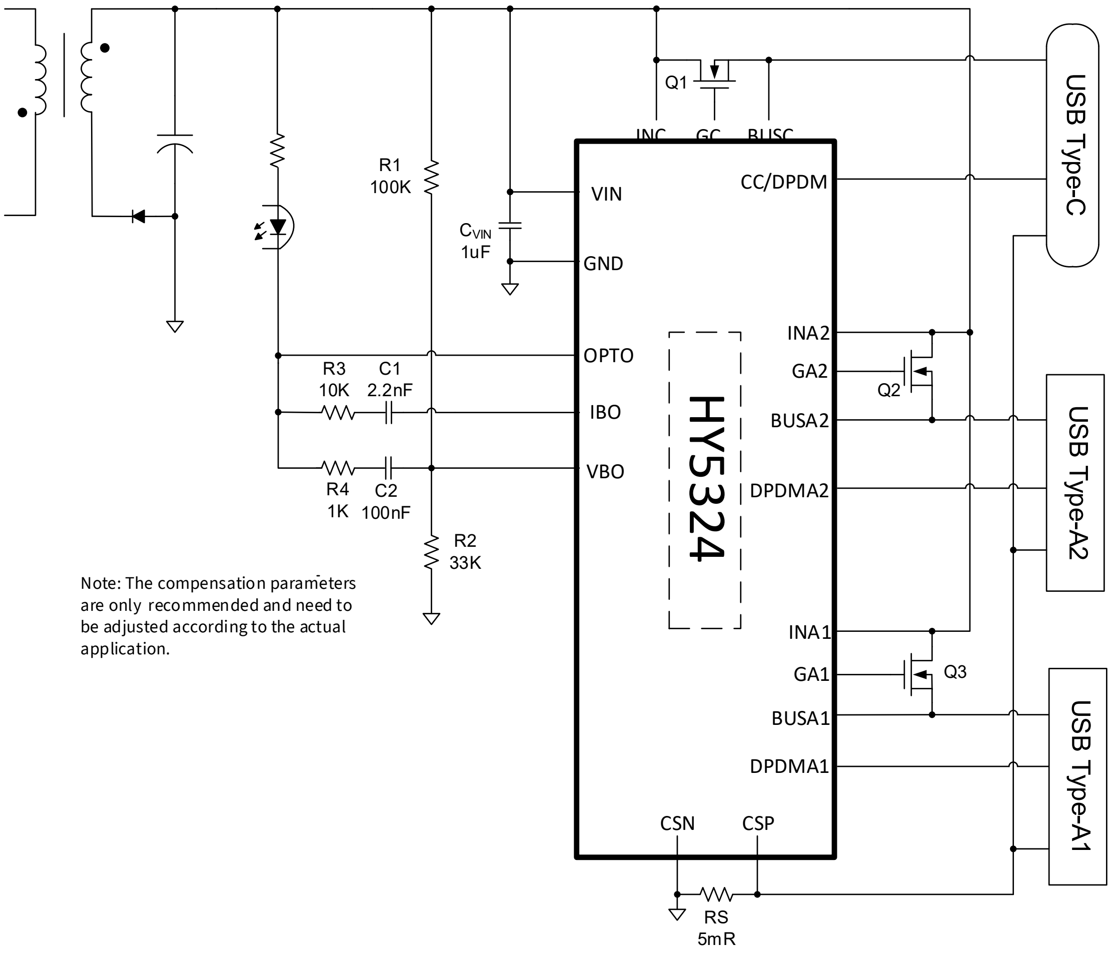
The HY5324 is a high performance, high integration USB Type-C Power Delivery and Type-A multi Ports Controller. The HY5324 supports 7 PDOs with programmable current and voltage which are fully compliant with USB Power Delivery Specification Revision 3.1, Version 1.8. Besides, the HY5324 also supports BC1.2 DCP, Apple 2.4A, QC2.0/QC3.0/QC3.0+, AFC, FCP, SCP, UFCS and PE+1.1/ 2.0 protocols.

The HY5324 designed for multi ports controller, which can easily uses to 1C2A application. Each port operates independently in fast charging mode and power is shared when both or more ports-working.

The HY5324 integrates Power-Link technology, making it easy to achieve multi ports power shared application.

The HY5324 integrates perfect protection such as Over Voltage Protection (OVP), Under Voltage Lockout (UVLO), Over Current Protection (OCP), Output Short Protection, CC or DPDM Over Voltage Protection and Over-temperature Protection.

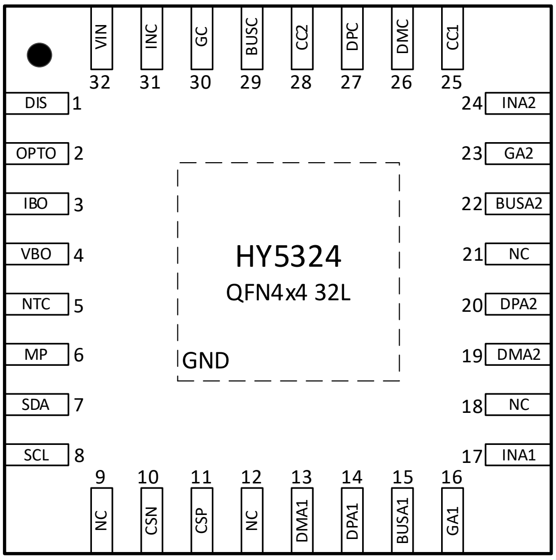
The HY5324 is available in QFN-32L (4 mmx4 mm) package.



Note: The compensation parameters are only recommended and need to be adjusted according to the actual application.

Fig. 1.Typical Application Schematic

4 Pin Configurations and Function Descriptions



QFN-32L (4 mmx4 mm)

Fig. 2. Packages Top View

Table 1. Pin Function Descriptions

Pin	Name	Description
1	DIS	External discharge loop control, could connect a resistor to VIN when used. When used for car charging, it can be used as bus voltage detection
2	OPTO	Optical coupler
3	IBO	Current feedback compensation
4	VBO	Output voltage feedback and compensation
5	NTC	An external negative temperature coefficient resistor connected to this pin for remote temperature sensing
6	MP	Communication with another chip through this pin if Power link function enable. If not used must tie to GND net
7	SDA	I2C BUS Data
8	SCL	I2C BUS Clock
9	NC	NC
10	CSN	Current detection negative point
11	CSP	Current detection positive point
12	NC	NC
13	DMA1	USB Type-A1 DM
14	DPA1	USB Type-A1 DP
15	BUSA1	USB Type-A1 VBUS voltage sense
16	GA1	External N-MOSFET gate control of USB Type-A1 VBUS power path
17	INA1	Power supply voltage sense for USB Type-A1
18	NC	
19	DMA2	USB Type-A2 DM

Pin	Name	Description
20	DPA2	USB Type-A2 DP
21	NC	
22	BUSA2	USB Type-A2 VBUS voltage sense
23	GA2	External N-MOSFET gate control of USB Type-A2 VBUS power path
24	INA2	Power supply voltage sense for USB Type-A2
25	CC1	Configuration channel interface pin to USB Type-C
26	DMC	USB Type-C DM
27	DPC	USB Type-C DP
28	CC2	Configuration channel interface pin to USB Type-C
29	BUSC	USB Type-C VBUS voltage sense
30	GC	External N-MOSFET gate control of USB Type-C VBUS power path
31	INC	Power supply voltage sense for USB Type-C
32	VIN	Power supply for internal circuits and the input voltage sense
EP	GND	Ground

5 Specification

5.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Unit
VBO, IBO, CSN, CSP, NTC, MP, SDA, SCL,	-0.3	6.5	V
CC1, CC2, DPC, DMC, DPA1, DMA1, DPA2, DMA2	-0.3	26	V
VIN, INC, BUSC, BUSA1, INA1, BUSA2, INA2, OPTO, DIS	-0.3	28	V
GC, GA1, GA2	-0.3	30	V
Junction Temperature Range	-40	150	°C
Ambient Temperature Range	-40	85	°C
Storage Temperature Range	-55	150	°C
Lead Temperature Range (Soldering 10 sec)		260	°C
ESD Human Body Model (100pF Capacitance, Series 1.5KΩ)	-4000	+4000	V

Note: Exceeding the specified limits for the operating conditions of the device can result in permanent damage to the device. The parameters provided are only the limit values for the operating conditions, and operating the device outside of the recommended working conditions is not advisable. The device's reliability may be affected by prolonged operation under extreme conditions.

5.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Min	Max	Unit
Input Voltage VIN	3	24	V
Junction Temperature Range	-40	150	°C

5.3 Electrical Characteristics

V_{in} = 5 V, T_{AMB} = 25 °C (unless noted otherwise)

Table 4. Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
VIN						
V_{IN}	Input Voltage		3		24	V
V_{IN_UVLO}		Rising		3.27		V
$V_{IN\_UVLO\_HYS}$	Input Under-Voltage Lockout(UVLO)			0.2		V
I_Q	Input Quiescent Current	CC Locked		3		mA
		CC Unlocked		200		uA
VOUT						
V_{OVP_TH}	V_{OUT} = 5V	For fixed PDO. For the continuous mode, it will select the threshold based on the range		6		V
	V_{OUT} = 9V			10.5		V
	V_{OUT} = 12V			13.8		V
	V_{OUT} = 15V			17.8		V
	V_{OUT} = 20V			24		V
Discharge						
I_{DIS}	Discharge Current	VOUT=20V			130	mA
R_{VBUS}	Bleeding resistor			100		kΩ
BMC Transmitter (CC1, CC2)						
$_z$Driver	TX Output Impedance		30	54	70	Ω
V_{Swing}	BMC Amplitude		1.050	1.125	1.200	V
V_{TXLOW}	Transmit LOW				75	mV
$f_{BitRate}$	BMC Rate		270	300	330	kbps
BMC Receiver (CC1, CC2)						
V_{RXHI}	Receiver HIGH	Rising edge		840		mV
V_{RXLOW}	Receiver LOW	Falling edge		530		mV
Type-C DFP specification (CC1, CC2)						
V_{D_SRC3A}	Detach threshold when detached in 3A DFP mode	Rising threshold	2.5	2.625	2.75	V
		Hysterias		0.05		V
V_{Rd_SRC3A}	Ra, Rd detection threshold in 3A mode (falling)	0V $\leqslant V_{CCx} \leqslant$ 2.5V	0.75	0.79	0.83	V
		Hysterias		0.02		V
I_{RP_SRC}	CC1/CC2 Broadcasting current	3A DFP, R_D=5.1K	1.6	1.68	1.76	V
$T_{CCDebounce}$	Deglitch filter for UFP attach detection		120	150	180	ms
$T_{PDDebounce}$	Deglitch filter for UFP detach detection		12	15	18	ms
Constant Current						
CC	Constant current point	Configurable				
SOCP	Short current protection	Rsense=5mΩ		16		A
HVDCP interface (DP, DM)						
V_{DAT_REF}	Data threshold voltage		0.25	0.325	0.4	V

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$T_{DP\_DEGLTICH\_HIGH}$	Denounce time for DP high detection			1.1		s
$T_{DM\_DEGLTICH\_LOW}$	Denounce time for DM low detection			1		ms
T_{VOUT_CHG}	Denounce time for VOUT variation		20	40	60	ms
R_{DP_LKG}	DP Leakage resistor			650		kΩ
R_{DM_DWN}	DM Pull down resistor			20		kΩ
V_{TH_PD}	Device connection threshold		0.25	0.325	0.4	V
TD_{PD}	Debounce time for device connection detection		120	160	200	ms
ΔI_{UP}	Voltage step up current	R1= 100 kΩ		0.2		µA
ΔI_{DOWN}	Voltage step down current	R1 = 100 kΩ		0.2		µA
T_{DUR_STEP}	Step time for continuous mode	QC3.0 mode		120		µs
Apple 2.4A Mode						
V_{DAT_2P7}	VDP/VDM	Apple 2.4A mode Voltage	2.57	2.7	2.84	V
UFCS Mode						
$V_{U\_TX\_VOH}$	UFCS TX valid high		2.56	3.3	3.6	V
$V_{U\_TX\_VOL}$	UFCS TX valid low				0.5	V
$V_{U\_RX\_VOH}$	UFCS RX valid high		1.4			V
$V_{U\_RX\_VOL}$	UFCS RX valid low				0.99	V
FCP mode						
V_{TX_VOH}	DM FCP TX valid high		1.8			V
V_{TX_VOL}	DM FCP TX valid low				0.3	V
V_{RX_VOH}	DM FCP RX valid high			1.2		V
V_{RX_VOL}	DM FCP RX valid low			0.9		V
UI	Unit interval for PHY	F_{CLK} = 125 kHz	144	160	176	µs
NTC						
I_{NTC}	NTC source current			48		µA
V_{NTC_TH}	NTC Protection Threshold	Rising		0.6		V
		Falling		0.3		V
V_{NTC_HYS}		Hysterias		0.3		V
OTP						
T_{J1}	Over temperature protection	Rising edge		145		°C
		Hysteresis		20		°C
I2C						
F_{I2C}	Bit rate				400	KHz

6 Function Description

6.1 Overview

The HY5324 is a high performance, high integration USB Type-C Power Delivery and Type-A multi Ports Controller. The HY5324 supports 7 PDOs with programmable current and voltage which are fully compliant with USB Power Delivery Specification Revision 3.1, Version 1.8. Besides, the HY5324 also supports BC1.2 DCP, Apple 2.4A, UFCS, QC2.0/QC3.0/QC3.0+, AFC, FCP, SCP and PE+1.1/2.0 protocols. It is an ideal solution for power supply devices liking quick charger adapters, and smart power strips.

The HY5324 integrates the CV and CC loop control, to eliminate TL431, so that the BOM is minimized.

A current sampling resistor is connected to a 5mΩ alloy resistor on CSN and CSP for current sampling.

The output voltage of the HY5324 has a programmable line compensation function. After the output current increases, the output voltage will be correspondingly increased to compensate for the voltage drop caused by the connection line impedance. For specific configuration requirements, please contact HYASiC.

The HY5324 has multiple protection functions, including output over-voltage protection, output short circuit protection, data pin short circuit protection, over-current protection and over-temperature protection.

6.2 Function Block

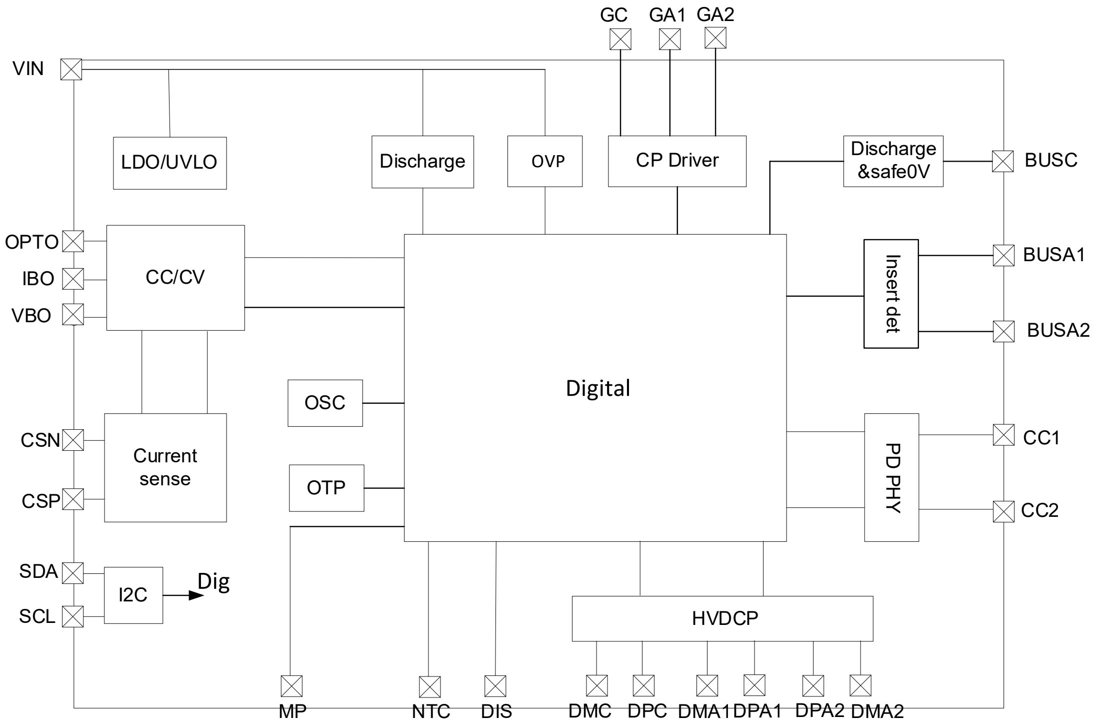


Fig. 3. Function Block

7 Application Notes

7.1 VIN PIN & BUSC PIN & BUSA

The VIN pin is the chip's internal power supply input and voltage sense input, connected to the AC-DC or DC-DC output, it is recommended to connect an external 1uF capacitor to GND near this pin. It is also an internal discharge drain pathway. Used to drain the charge stored by the output capacitor of the external AC/DC power supply when the device is removed or the device requests a step-down, so that the voltage is regulated to safe 5V or the target voltage.

The BUSC pin is used to sense the USB Type-C port voltage, and is also used as a USB Type-C port Discharge path, and it is recommended to connect an external 1uF capacitor to GND.

The BUSA pin is used to sense the USB Type-A port voltage, and connects to the external N-MOSFET Source. This pin is also used to detect whether there is a device inserted on USB Type-A receptacle side. The capacitance connected BUSA PIN to GND is not allowed.

7.2 GC PIN & GA PIN

The GC pin and GA pin are used to drive the external NMOS FET of the power path, connected to the gate of the NMOS FET. When the HY5324 detects that a device is connected or removed, it controls NMOS to turn on or off. When a fault occurs, the NMOS will be quickly turned off to protect the device and improve safety.

7.3 MP PIN

This pin is used to perform communication between two chips if Power-Link function enable.

7.4 Constant Voltage and Constant Current

The HY5324 integrates CV and CC loop control. As shown in the figure below, CV loop control is realized through VBO and OPTO, where OPTO is connected to an external optocoupler and VBO is connected to a voltage divider network point composed of R1 and R2. When the device requests a voltage to step-up or step-down, the HY5324 feeds back the network node according to sink or source current in 0.2uA/step through VBO. Whether it is VBO feedback or OPTO feedback, R1 must be 100K, R2 is 33K in OPTO feedback applications, and R2 is calculated based on the actual situation of the front-end power supply in FB feedback applications.

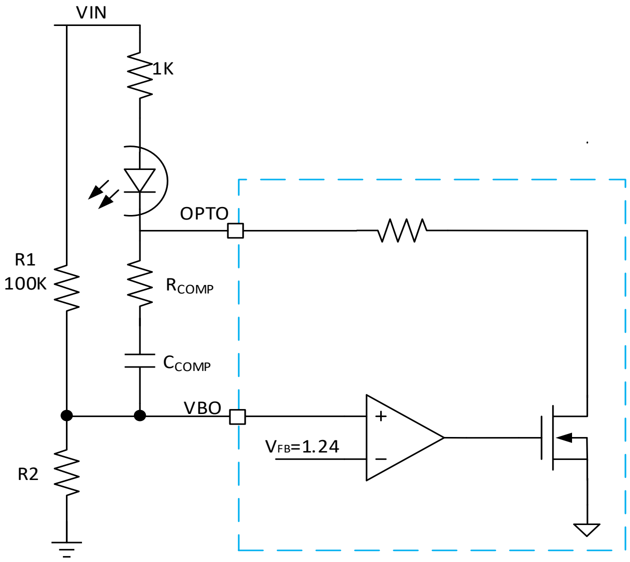


Fig. 4. OPTO Feedback

To suppose the input voltage is VIN, and VBO of the power source is regulated to V_{FB}, then there is how to calculate the resistance of R2:

$$R2 = \frac{V_{FB} \times \mathrm{R1}}{\mathrm{VIN} - V_{FB}}$$

Equation 1

The HY5324 implements constant current control and current sampling via OPTO, IBO, and CSN and CSP with an external sampling resistor of 5mΩ. The sampling resistor should be layout in Kelvin connection, with one end being the CSP and the other end being the CSN of the chip. The sampled current information is also used by the HY5324 to determine whether is over current or short circuit. The compensation network between OPTO and IBO needs to be adjusted for the specified application.

7.5 Line-Drop compensation

The Built-in line drop compensation function of the HY5324 has programmable compensation coefficient to meet different application, according to output current. The HY5324 currently supports five types of line drop compensation coefficients: 0mV/A, 50mV/A, 100mV/A, 150mV/A, 200mV/A. The default configuration is 100mV/A.

7.6 NTC Protection

The HY5324 uses the NTC pin to sense the external temperature. As show in Fig.5, there is an internal current source 48 µA at the NTC pin. With an external NTC resistor from NTC pin to ground, the HY5324 can detect the voltage across this NTC resistor and calculate the temperature per the T-R characteristics. When the NTC PIN is used to power reduction function, the threshold is 0.6V, when it used to protection function, the rising threshold is 0.6V and the falling threshold 0.3V.

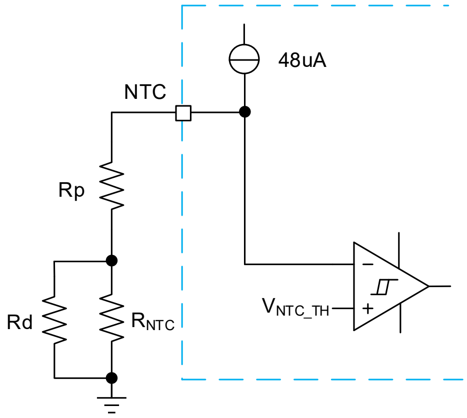


Fig. 5. NTC Protection

7.7 Over Voltage Protection

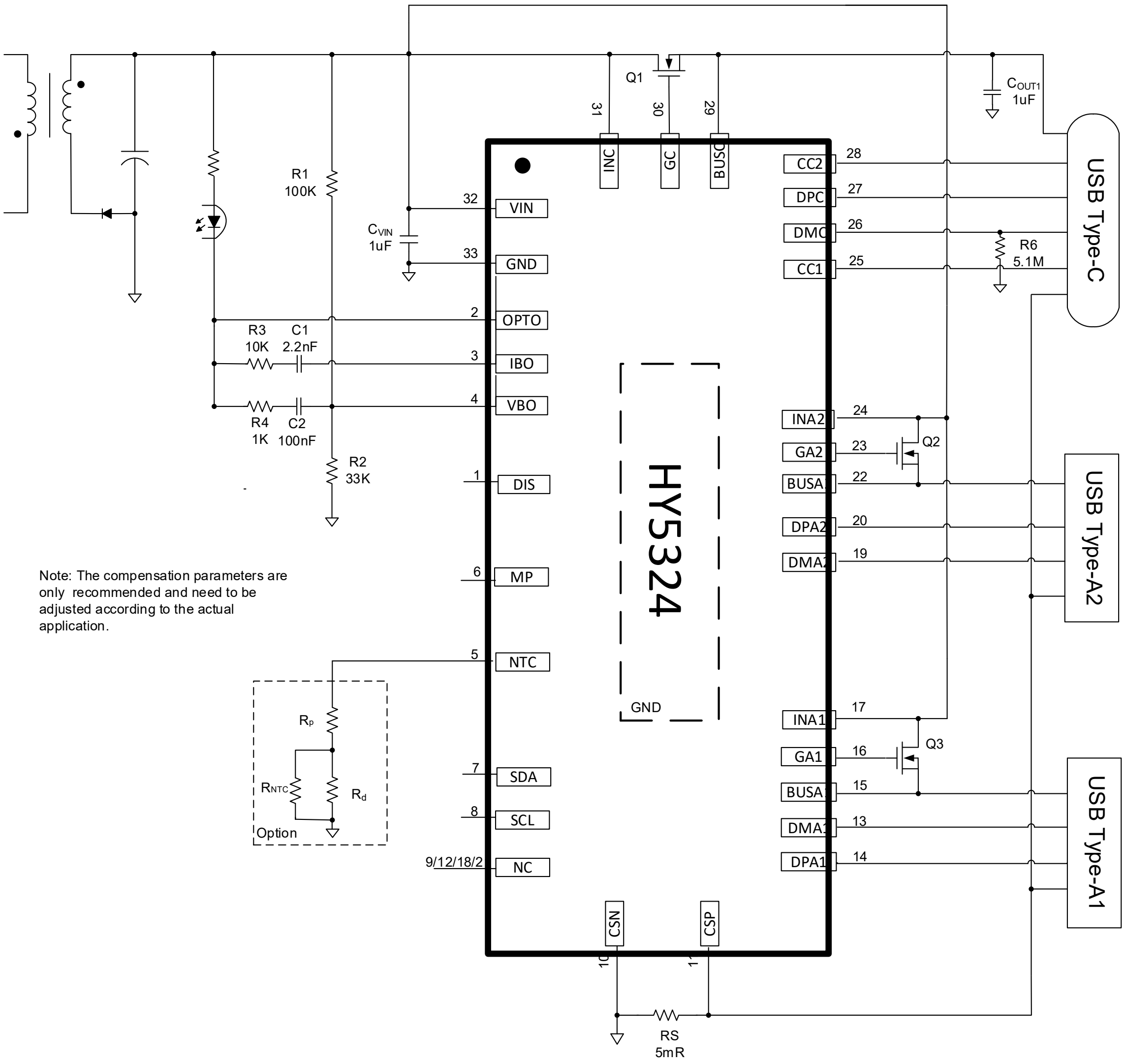
The HY5324 supports OVP by monitoring the voltage of VIN pin, once the voltage exceeds the over voltage threshold of the required the OVP procedure will be triggered, and then the HY5324 turns off external NMOS FET quickly.

7.8 OCP and short protection

The HY5324 monitors output current through the external 5mΩ sense resistor connected to CSP and CSN for over current and short-circuit protection. When the output current exceeds the over current protection threshold or short-circuit protection threshold corresponding to the requested, the over current or short-circuit protection procedure is triggered, and then the HY5324 turns off external NMOS FET quickly.

8 Typical Application Circuit

8.1 AC/DC - OPTO feedback



Note: The compensation parameters are only recommended and need to be adjusted according to the actual application.

Fig. 6. 1C2A Application for OPTO feedback

Note:

1, Must using Kelvin Connect to connect current sense resistor RS, NMOS Q1, NMOS Q2, NMOS Q3.

2, If there are high requirements for electrostatic protection, it is recommended to connect a resistor (33 Ω) in series and a capacitor (330 pF) in parallel on the communication pin.

3, The capacitor C1’s value shall not more than 10nF.

4, The C_{VIN} must near the VIN pin and uses a single route connect to the VIN net will be better for EMI.

8.2 DC/DC - FB feedback

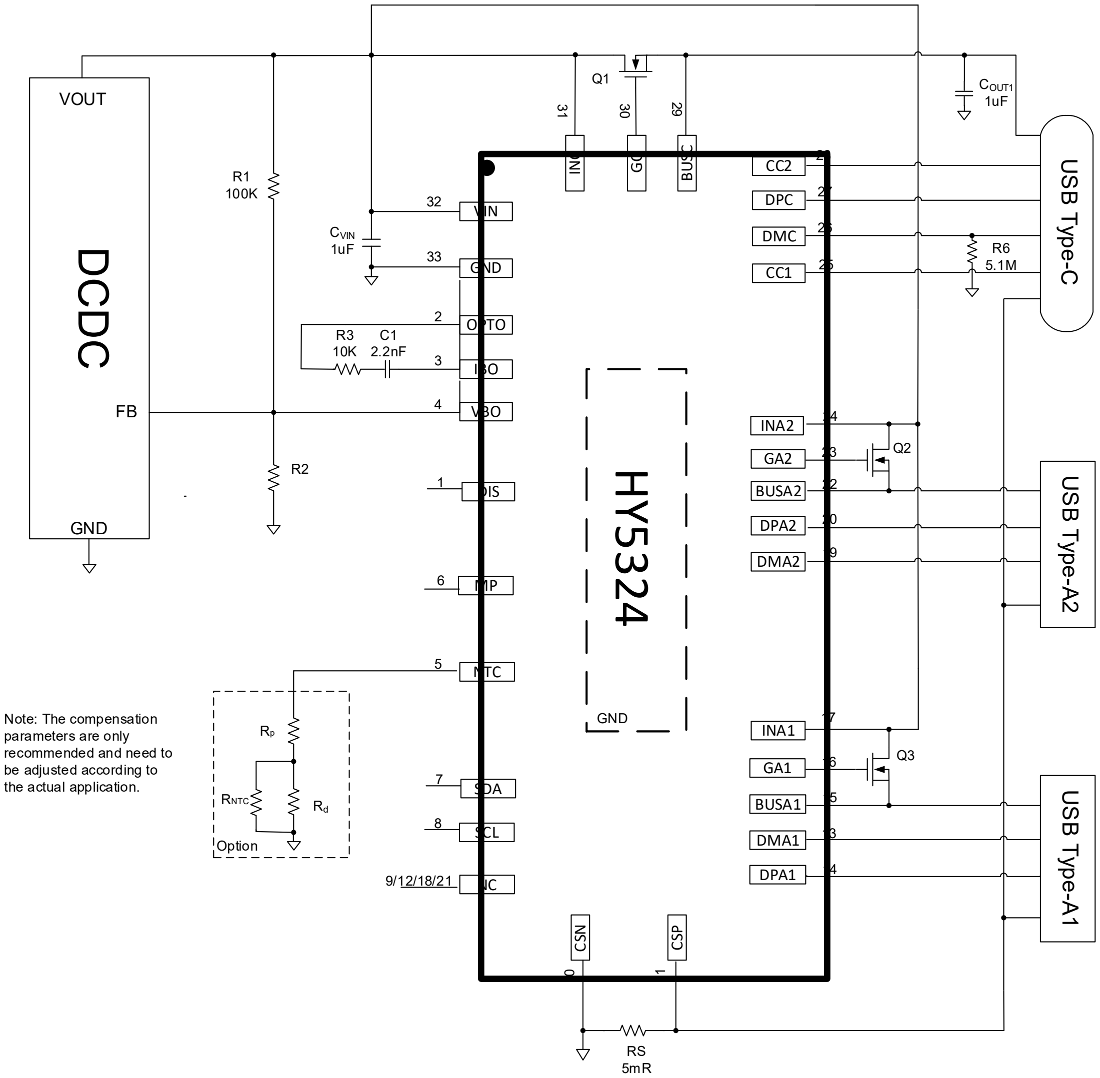


Fig. 7. 1C2A Application for FB feedback

Note:

1, Must using Kelvin Connect to connect current sense resistor RS, NMOS Q1, NMOS Q2, NMOS Q3.

2, If there are high requirements for electrostatic protection, it is recommended to connect a resistor (33 Ω) in series and a capacitor (330 pF) in parallel on the communication pin.

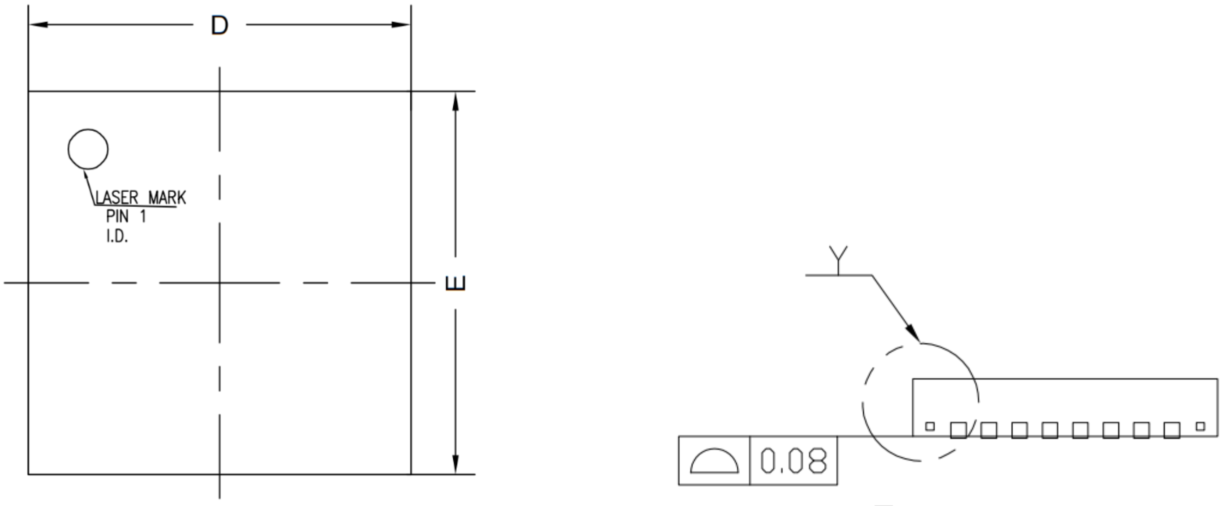
3, The R2’s value calculated from the FB feedback voltage.

4, The capacitor C1’s value shall not more than 10nF.

5, The C_{VIN} must near the VIN pin and uses a single route connected to the VIN net will be better for EMI.

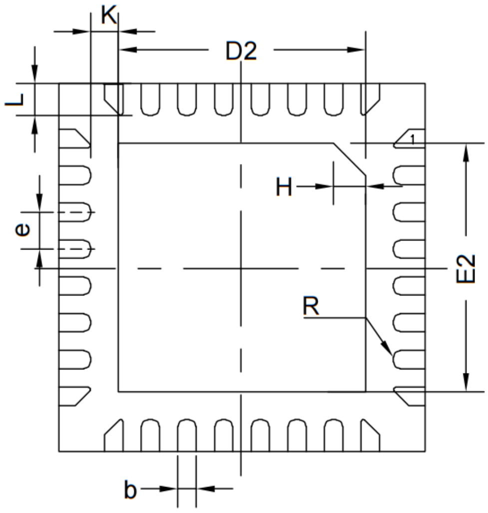
9 Mechanical, Packaging & Orderable Info

9.1 Package Outline: QFN 4 mm X 4 mm-32L



Top View

Side View



Bottom View

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e		0.40BSC	
K		0.30REF	
H		0.35REF	
L	0.275	0.35	0.425
R		0.075REF	

Legend

QFN 4 mm X 4mm-32L

Fig. 8. Package Outline

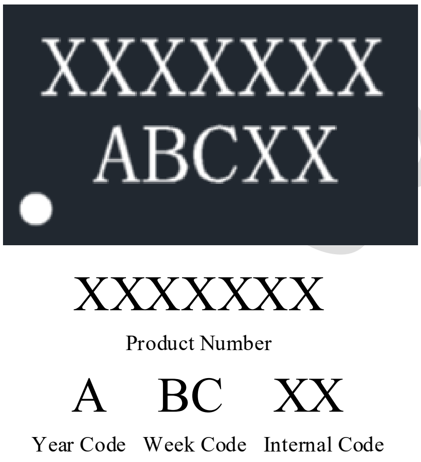
9.2 Ordering Information

Part Number	Configuration	Package	MOD
HY5324B20001Q	FPDO:5V/3A,9V/2.22A,12V/1.67A	QFN-32L	6K/Reel
	PPS:5-11V/2A		
	QC2.0/QC3.0/QC3.0+(class A)/FCP/SCP/AFC/APPLE 2.4A/BC1.2		
	Line drop compensation:100mV/A		
	OCP:115%		
HY5324D30001Q	FPDO:5V/3A,9V/3A,12V/2.5A,15V/2A,20V/1.5A	QFN-32L	6K/Reel
	PPS:5-11V/3A,5-16V/2A		
	QC2.0/QC3.0/QC3.0+(class A)/FCP/SCP/AFC/APPLE 2.4A/BC1.2		
	Line drop compensation:100mV/A		
	OCP:115%		
HY5324XXXXXXX	For part numbers not listed above, please contact Hyasic		

9.3 Tape and Reel Information

Package Type	PCs/Reel	Reel/Reel Box	Reel Box/Carton Box	PCs/Carton Box
QFN 4X4-32L	6K	1	5	30K

9.4 Marking and Date Code Information



Year		Year Code
2009	2024	A
2010	2025	B
2011	2026	C
2012	2027	D
2013	2028	E
2014	2029	F
2015	2030	G
2016	2031	H
2017	2032	J
2018	2033	K
2019	2034	L
2020	2035	M
2021	2036	N
2022	2037	P
2023	2038	Q

10 Revision History

Revision	Date	Changes
0.1	2024-03-31	Brief datasheet
0.2	2024-04-12	Initial datasheet
1.0	2024-09-26	Update Junction Temperature Range 150 °C Update the Revision to 1.0

11 Important Notice

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12 Contact Information